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APPLICATION FOR LETTERS PATENT

for

**METHOD FOR STABILIZING  
HIGH PRESSURE OXIDATION OF A SEMICONDUCTOR DEVICE**

Inventors:  
F. Daniel Gealy  
Dave Chapek  
Scott DeBoer  
Husam N. Al-Shareef  
Randhir Thakur

Attorney:  
James R. Duzan  
Registration No. 28,393  
TRASKBRITT, PC  
P.O. Box 2550  
Salt Lake City, Utah 84110  
(801) 532-1922

## TITLE OF THE INVENTION

### METHOD FOR STABILIZING HIGH PRESSURE OXIDATION OF A SEMICONDUCTOR DEVICE

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a continuation of application Serial No. 10/212,892, filed August 5, 2002, pending, which is a continuation of application Serial No. 09/798,445, filed March 2, 2001, pending, which is a divisional of application Serial No. 09/386,941, filed August 31, 1999, now U.S. Patent 6,291,364, issued September 18, 2001.

## BACKGROUND OF THE INVENTION

**[0002]** The present invention relates generally to oxidizing a semiconductor surface during an anneal processing step and, more particularly, the present invention relates to stabilizing a high pressure oxidation step using nitrous oxide gas within a temperature range of 600° to 750°C.

**[0003]** Advanced semiconductor devices, such as high density dynamic random access memories ("DRAMs"), impose severe restrictions on the times, temperatures, and atmospheres of all thermal process steps. DRAMs are comprised of a plurality of memory cells. Each memory cell is further comprised of a field effect transistor and a capacitor. It is well known in the art of semiconductor fabrication to use planar capacitors within DRAM cells; however, in DRAM cells that utilize conventional planar capacitors, more integrated circuit surface area is dedicated to the planar capacitor than to the field effect transistor.

**[0004]** As the density of components in integrated circuit memories increased, the shrinkage of memory cell size resulted in a number of other problems in addition to the problems associated with a smaller capacitor. Among the resulting problems was that of dopant diffusing out of the semiconductor material when forming the transistors of the memory cells. In order to form transistors, dopants must be implanted in regions of the semiconductor materials. The dopant, however, tends to diffuse out of the transistor regions when the transistors are heated

during subsequent integrated circuit processing steps. For example, dopant diffuses from the semiconductor material during the reoxidation anneal of the dielectric layer of the cell capacitor.

[0005] Silicon nitride is used as a dielectric layer because it has less desirable leakage current properties than silicon dioxide. Further, a thin oxide layer is grown upon the dielectric layer by reoxidizing a layer of silicon nitride enough to form this oxide layer to further reduce the leakage current of the silicon nitride film.

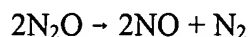
[0006] Once the proper amount of silicon oxide and nitride oxide have been grown upon the surface to form the dielectric layer, a reoxidation anneal step is necessary to reduce the imperfections typically occurring during the initial reoxidation growth stages.

[0007] One method to provide the silicon dioxide film is to perform a high pressure chemical vapor deposition (HVCVD) process step on the semiconductor device. The formation of the cell dielectric, as well as transistor gate oxides and reoxidation steps in other processing application steps, is subjected to high pressures in excess of one atmosphere, typically between five (5) atmospheres to twenty-five (25) atmospheres, where an atmosphere is represented as a pressure of 760 Torr. An atmosphere of pure  $N_2O$  is introduced under such pressures in a temperature range of 600°C. to 800°C. The desired reaction is:



This allows the oxygen to react with the silicon surface, forming the silicon dioxide layer.

[0008] Unfortunately, as the  $N_2O$  reaction proceeds, it can become uncontrollable under certain circumstances; specifically, the  $N_2O$  reaction can become supercritical, which gives rise to high pressure spikes within the high pressure oxidation furnace. These high pressure spikes abort the high pressure furnace runs and prevent the furnaces from operating in pure  $N_2O$  in the temperature range of 600°C. to 750°C. As the concentration of unreacted  $N_2O$  builds up in the high pressure oxidation furnace, it reaches a critical point where the disassociation reaction is self-propitiating. This reaction goes from



Once the concentration of unreacted  $N_2O$  exceeds this critical point, the uncontrolled reaction occurs and generates pressure spikes that may explode a furnace tube of the high pressure

oxidation furnace. An exploding furnace tube results in ruined product as well as dangerous working environment conditions for personnel.

[0009] Accordingly, a method and apparatus is needed that reduces, if not, prevents the unreacted N<sub>2</sub>O from becoming super critical to ensure the uniform processing of the semiconductor wafers.

#### BRIEF SUMMARY OF THE INVENTION

[0010] According to the present invention, a method and apparatus for preventing N<sub>2</sub>O from becoming super critical during a high pressure oxidation stage within a high pressure oxidation furnace are disclosed. The method and apparatus utilize a catalyst to catalytically disassociate N<sub>2</sub>O as it enters the high pressure oxidation furnace. This catalyst is used in an environment of between five (5) atmospheres to twenty-five (25) atmospheres N<sub>2</sub>O and a temperature range of 600° to 750°C., which are the conditions that lead to the N<sub>2</sub>O going super critical. By preventing the N<sub>2</sub>O from becoming super critical, the reaction is controlled that prevents both temperature and pressure spikes. The catalyst can be selected from the group of noble transition metals and their oxides. This group can comprise Palladium, Platinum, Iridium, Rhodium, Nickel, Silver, and Gold.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 depicts a block diagram of a high-pressure furnace with a catalytic matrix sleeve inserted therein;

[0012] FIG. 2 depicts a grid arrangement of the catalytic matrix sleeve used in FIG. 1; and

[0013] FIG. 3 depicts a high pressure furnace that uses a catalytic matrix screen in an alternative embodiment.

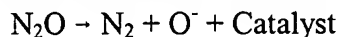
#### DETAILED DESCRIPTION OF THE INVENTION

[0014] With reference to drawing FIG. 1, a high pressure furnace 10 for chemical vapor deposition is illustrated. The furnace 10 comprises a reactor vessel or furnace tube 12 and a front

and rear flange assembly 14 and 16, respectively. Wafers are positioned within furnace tube 12. Front flange assembly 14 includes various gas inlets. The gas inlets terminate right at the flange assembly. Gas is injected into furnace tube 12 and immediately adjacent the inlet flange. An exhaust port 18 connects to a suitable pump for exhausting gases from furnace tube 12. Placed within furnace tube 12 is a catalyst matrix liner 20 that is comprised of a catalyst element that catalyzes  $N_2O$  gas dissociation as the gas enters the furnace tube 12.

[0015] Furnace 10 operates under high pressure and temperatures. The pressure is above one atmosphere and ranges from five (5) atmospheres to twenty-five (25) atmospheres. The temperature range is from  $600^{\circ}C.$  to  $750^{\circ}C.$  These pressures and temperatures can be greater or less, with a transition through the stated temperature range. The importance of using catalyst matrix liner 20 is to protect against pressure and temperature spiking occurring within the furnace tube 12 of the furnace 10 during such pressure and temperature ranges of operation of the furnace 10.

[0016] Catalyst matrix liner 20, which is also shown in drawing FIG. 2, is comprised of a catalyzing agent that causes the  $N_2O$  gas in the furnace 10 to react to form the base components of nitrogen and oxygen of the  $N_2O$  gas according to the following reaction:

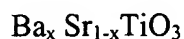


The use of the a catalyst constrains the chemical reaction from running away or becoming uncontrollable, which would cause a pressure and temperature surge within the furnace 10. Such surges must be avoided as they destroy the semiconductor materials under fabrication within the furnace 10 as well as causing the possible destruction of the furnace tube 12.

[0017] Catalyst materials are selected from the group consisting of Palladium, Platinum, Iridium, Rhodium, Nickel, and Silver. Gold also can be used as a catalyst, but should be avoided as gold contaminates the silicon used in the wafers on which semiconductor devices are formed. Additional catalysts include perovskites,  $CaTiO_3$ , a natural or synthetic crystalline mineral composed of calcium dioxide and titanium dioxide. When using a Tantalum compound to form the gate oxide or the cell dielectric for the transistors of a semiconductor device, a tantalum oxide is produced in the  $N_2O$  atmosphere in the furnace 10. The oxygen from the  $N_2O$  combines with the tantalum oxide according to the following reaction:



The use of the catalyst material helps to drive this reaction nearly to full stoichiometry. When used with the a Barium Strontium Titanate compound, the catalyst allows the oxidation to produce:



which is driven to full a stoichiometry reaction as well.

**[0018]** The catalyst matrix liner 20 of drawing FIG. 2 is shown to be in a honeycomb or hexagonal geometry. This particular geometry is used because of its ease of manufacture and its strength and stability. Other geometric shapes are also possible, such as, for example, circles, ovals, rectangles, diamonds, and other various types of polygonal shapes. Referring to drawing FIG. 3, illustrated is an alternative embodiment of catalyst matrix liner 20 with respect to its location within furnace 10. In this embodiment, catalyst matrix liner 20 is placed next to the gas inlets of front flange assembly 14. This position allows for the nitrous oxide to strike the catalyst matrix liner 20 as the gas enters the furnace chamber or tube 12 of furnace 10. Again, as stated previously, the contents of furnace 10 in drawing FIG. 3 are under high pressure and temperatures as described herein.

**[0019]** The catalyst matrix liner 20 can be made having a honeycomb or hexagonal base or supporting material base from a material, such as stainless steel, which is subsequently plated with the desired catalytic material as described herein. Other well known materials may be used for the honeycomb or hexagonal catalyst matrix liner that are suitable for such use as a substitute for stainless steel include aluminum oxide, or other suitable structural ceramics where the catalyst is embedded therein.

**[0020]** The furnace 10 is useful during gate oxidation in growing either a nitride layer or an oxide layer, or both. Further, cell dielectric layers can also be oxidized under safe conditions using the furnace 10. Additionally, reoxidation can be performed safely under the desired temperature and pressure constraints as described herein within the furnace 10. The advantages of using high pressures within the stated temperature range is that the semiconductor material is not subjected to the high heat loads of temperature in excess of 800°C., which can warp and damage the wafers as well as inhibit the oxide growth layer. Additionally, the reactions

within the furnace 10 can be easily controlled during operation without undesired reactions occurring. Additionally, the high pressure oxidation process minimizes the time the wafers are subjected to high temperatures and helps to minimize any undesirable diffusion of dopants whose rate of diffusion increases with increases in temperature.

**[0021]** While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.